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(54) **METHOD AND SYSTEM FOR IMPROVING DATA INTEGRITY IN NON-VOLATILE STORAGE**

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(52) **U.S. Cl.**

CPC ***H03M 13/2909*** (2013.01); ***G06F 11/1012*** (2013.01)

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None

See application file for complete search history.

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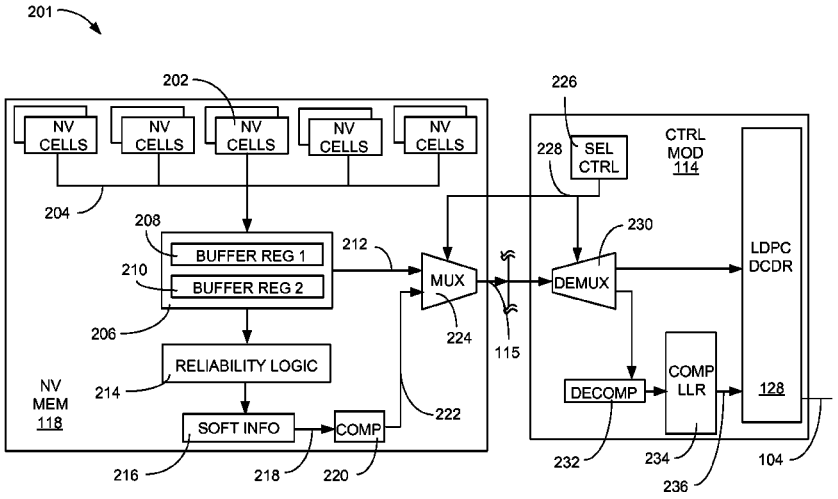
(57) **ABSTRACT**

A method for improving data integrity in a non-volatile memory system includes: accessing a non-volatile memory cell for retrieving hard data bits; generating soft information by capturing a reliability of the hard data bits; calculating syndrome bits by applying a lossy compression to the soft information; and generating a host data by executing a low density parity check (LDPC) iterative decode on the hard data bits and the syndrome bits.

15 Claims, 6 Drawing Sheets



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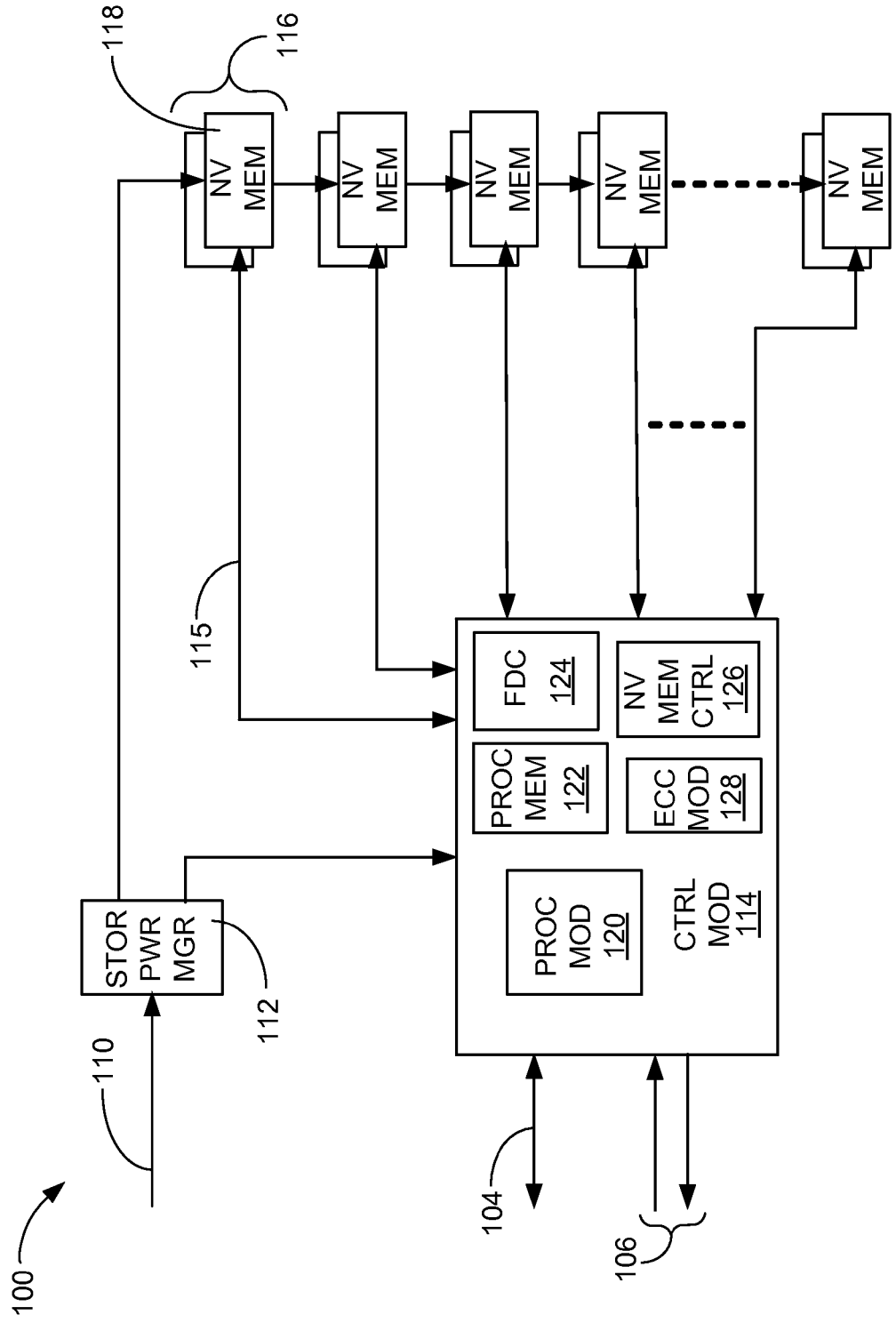
118
116
NV MEM
NV MEM
NV MEM
NV MEM
NV MEM
115
FDC 124
NV MEM CTRL 126
PROC MEM 122
ECC MOD 128
PROC MOD 120
CTRL MOD 114
STOR PWR MGR
112
110
104
106
100

FIG. 1

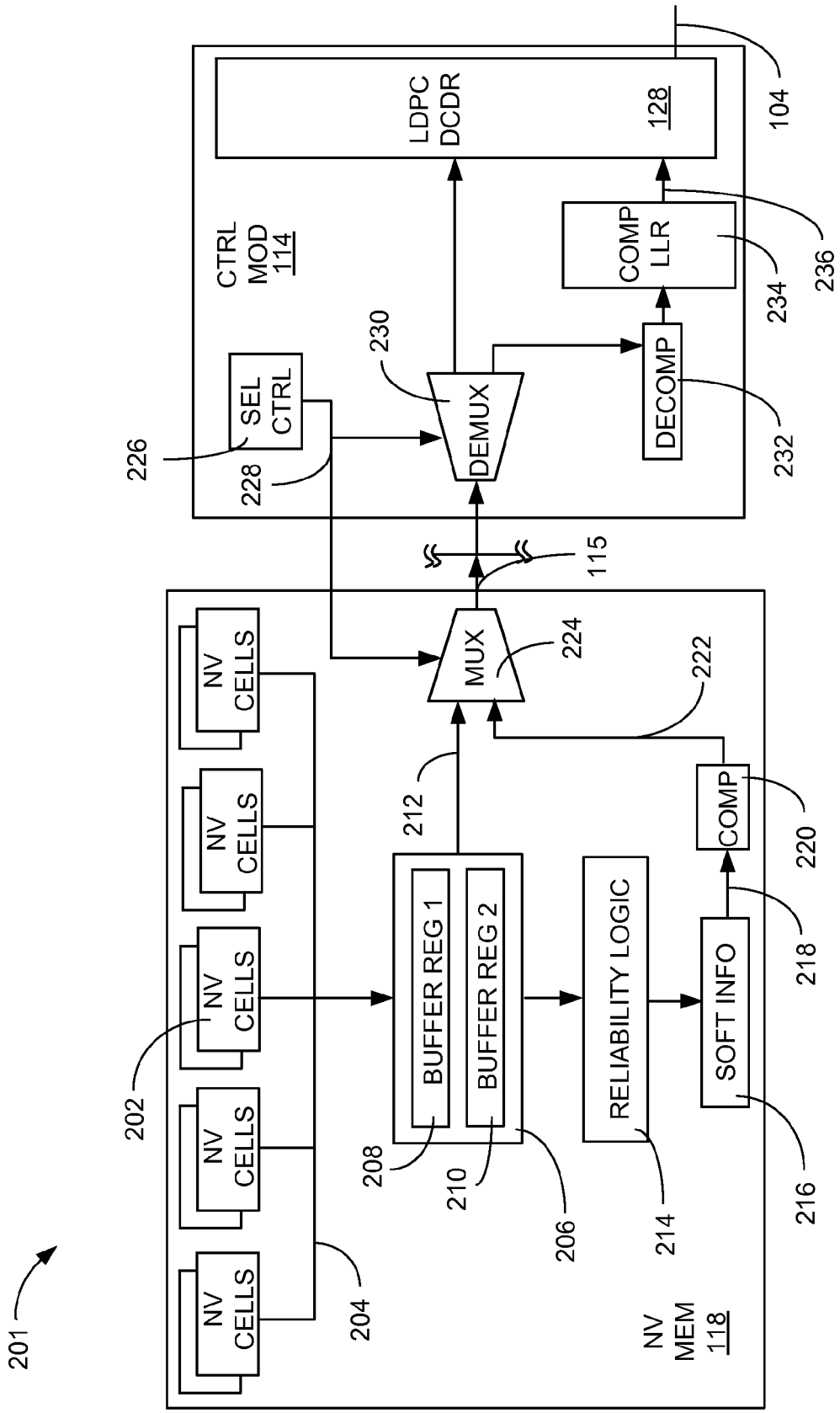
201
NV CELLS
NV CELLS
NV CELLS
NV CELLS
NV CELLS
202
204
NV MEM 118
BUFFER REG 1
BUFFER REG 2
208
210
206
212
RELIABILITY LOGIC
214
SOFT INFO
216
218
COMP
220
222
MUX
224
115
CTRL MOD 114
SEL CTRL
226
228
DEMUX
230
DECOMP
232
COMP LLR
234
236
LDPC DCDR
128
104

FIG. 2

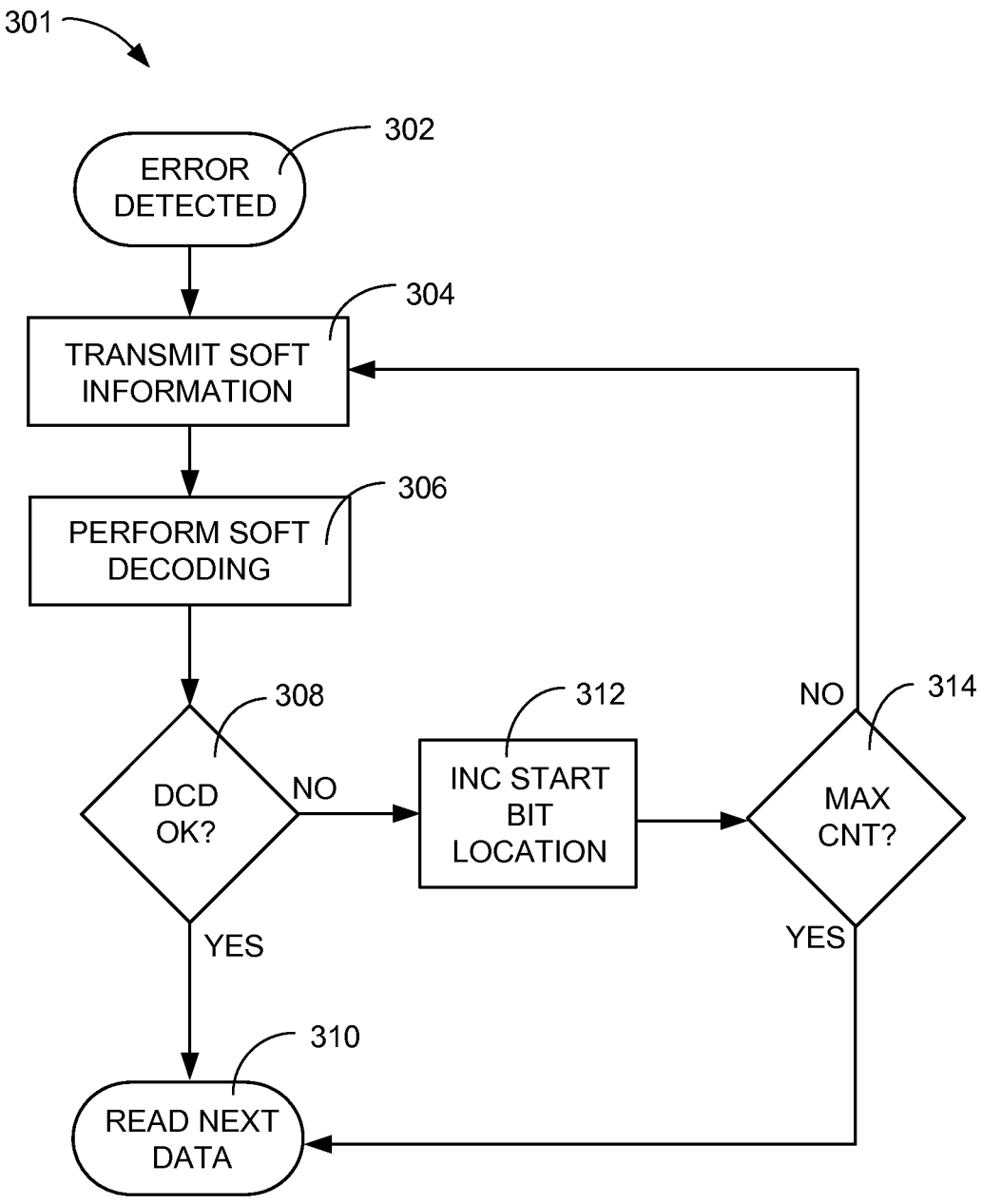
301
302
ERROR DETECTED
304
TRANSMIT SOFT INFORMATION
306
PERFORM SOFT DECODING
308
DCD OK?
NO
312
INC START BIT LOCATION
NO
314
MAX CNT?
YES
YES
310
READ NEXT DATA

FIG. 3

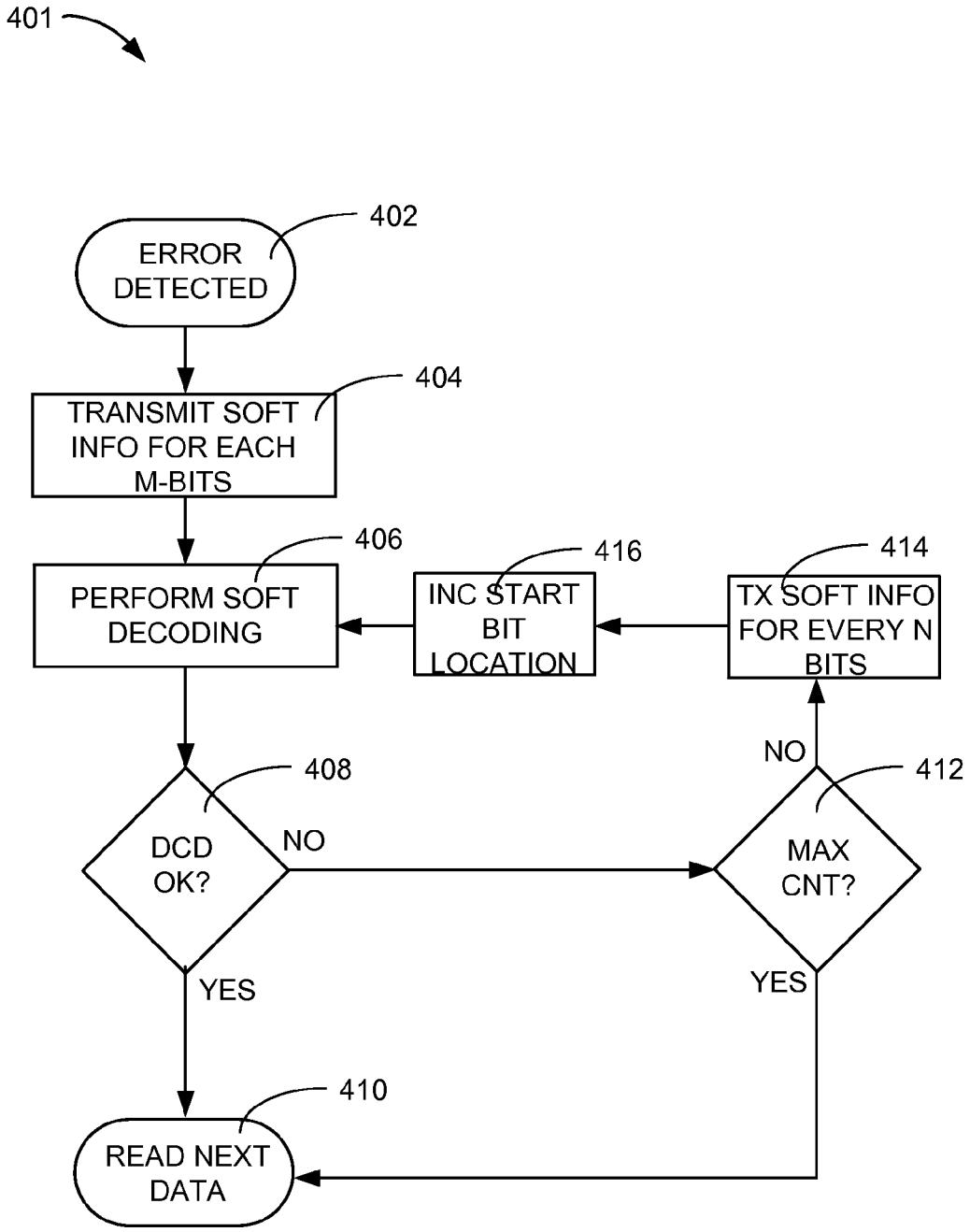
401
402
ERROR DETECTED
404
TRANSMIT SOFT INFO FOR EACH M-BITS
406
PERFORM SOFT DECODING
416
INC START BIT LOCATION
414
TX SOFT INFO FOR EVERY N BITS
408
DCD OK?
NO
412
MAX CNT?
NO
YES
YES
410
READ NEXT DATA

FIG. 4

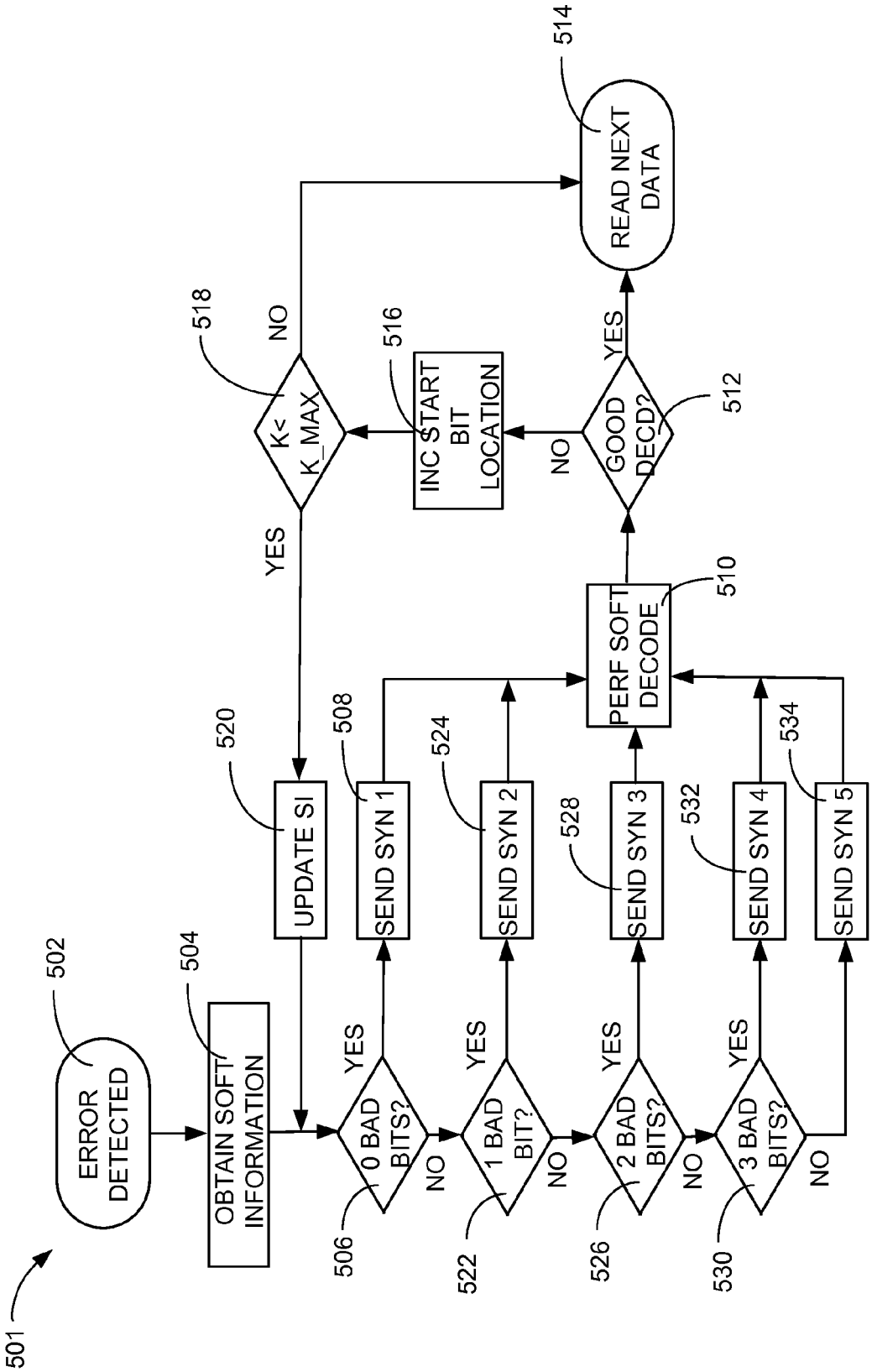
501
502
ERROR DETECTED
504
OBTAIN SOFT INFORMATION
506
0 BAD BITS?
508
SEND SYN 1
510
PERF SOFT DECODE
512
GOOD DECD?
514
READ NEXT DATA
516
INC START BIT LOCATION
518
K< K_MAX
520
UPDATE SI
522
1 BAD BIT?
524
SEND SYN 2
526
2 BAD BITS?
528
SEND SYN 3
530
3 BAD BITS?
532
SEND SYN 4
534
SEND SYN 5
YES
NO

FIG. 5

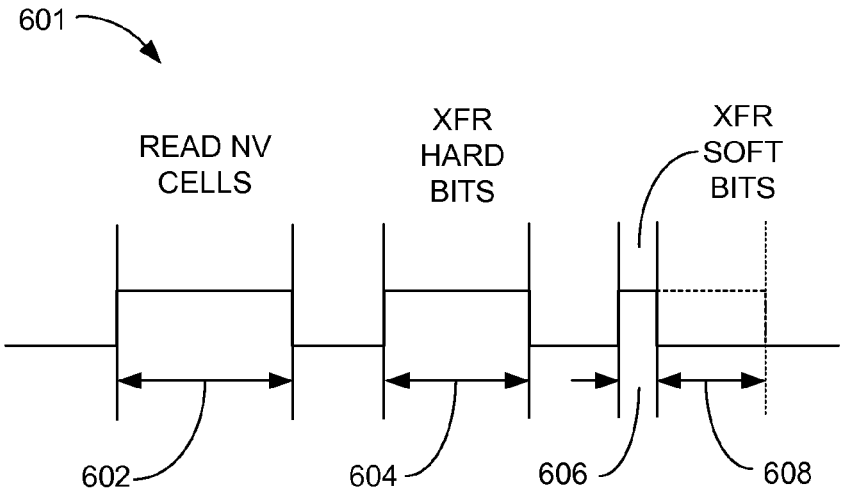
601
READ NV CELLS
XFR HARD BITS
XFR SOFT BITS
602
604
606
608

FIG. 6

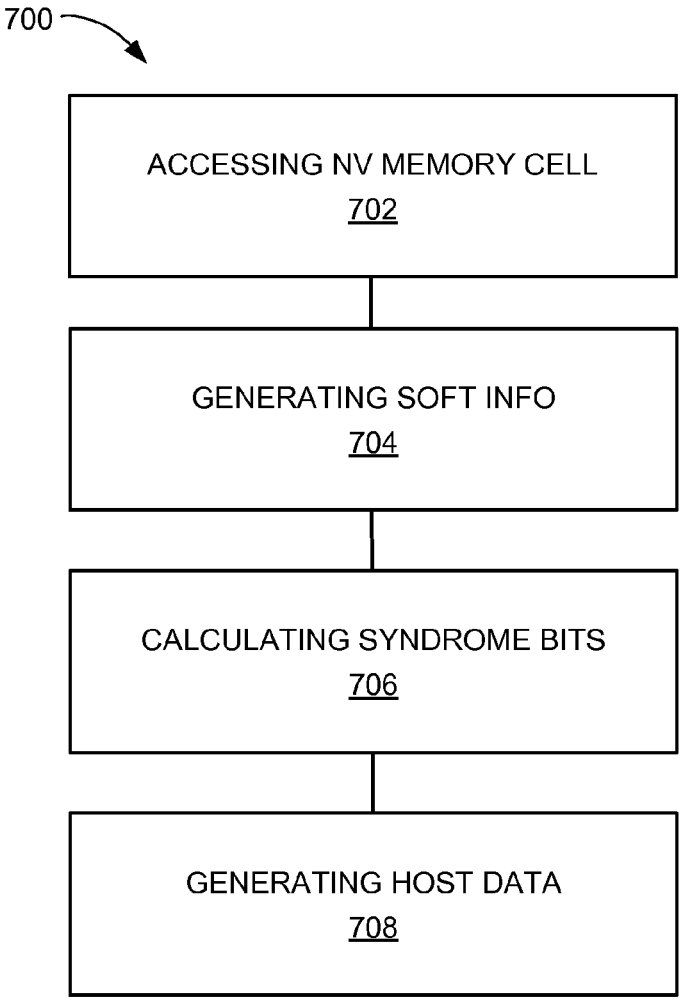
700
ACCESSING NV MEMORY CELL
702
GENERATING SOFT INFO
704
CALCULATING SYNDROME BITS
706
GENERATING HOST DATA
708

FIG. 7

METHOD AND SYSTEM FOR IMPROVING DATA INTEGRITY IN NON-VOLATILE STORAGE

CROSS REFERENCE TO RELATED APPLICATION

This application claims the benefit of U.S. Provisional Patent Application Ser. No. 61/767,234 filed Feb. 20, 2013, which is incorporated herein by reference in its entirety.

TECHNICAL FIELD

The present invention relates generally to a non-volatile memory system, and more particularly to a method for improving data integrity including with accessing memory using soft information.

BACKGROUND ART

Recently, there has been a growing demand for memory storage devices using NAND Flash memory due to their attractive features such as low power consumption, high data throughput, and small size. The original NAND flash architecture was referred to as single level cell (SLC) since it would only store one bit per in each memory cell (a floating gate transistor). More recent devices can store multiple bits per cell and are referred to as multi-level cell (MLC) flash.

In a solid state drive (SSD), a common requirement is that the drive maintains constant performance throughout its life. Some measures of performance are the operating power, the read throughput, and the average latency. In practice, reliability of the information stored in the flash decreases due to several factors such as cell-to-cell interference, charge leakage, over programming and read/write disturbance. These effects will become more severe with the age of the flash and the number of stored bits per cell. To resolve these issues, error correction codes (ECC) have been used to ensure data integrity and reliable data storage throughout the life of flash memory cells. By applying ECC, additional error correction bits are sent along the original data bits to protect the user data from errors caused by the weak or failing flash memory cells. Unfortunately, the addition of the error correction bits can reduce usable capacity. The fixed structure of the error correction codes can unnecessarily burden the storage capacity when no correction is necessary but can be insufficient to correct the user data as the flash memory cells wear.

Thus, a need still remains for a non-volatile memory system with error correction that can provide enhanced performance and longevity of a non-volatile storage system. In view of the growing market in the personal computer and peripheral areas, it is increasingly critical that answers be found to these problems. In view of the ever-increasing commercial competitive pressures, along with growing consumer expectations and the diminishing opportunities for meaningful product differentiation in the marketplace, it is critical that answers be found for these problems. Additionally, the need to reduce costs, improve efficiencies and performance, and meet competitive pressures adds an even greater urgency to the critical necessity for finding answers to these problems.

Solutions to these problems have been long sought but prior developments have not taught or suggested any solutions and, thus, solutions to these problems have long eluded those skilled in the art.

SUMMARY

The present disclosure provides a system and method of improving data integrity in a non-volatile memory system. In one implementation, improving data integrity can include accessing a non-volatile memory cell for retrieving hard data bits representing the user data. The non-volatile memory system generates soft information by capturing a reliability of the hard data bits without adding a capacity burden to the solid state drive. The non-volatile memory system calculates syndrome bits by applying a lossy compression to the soft information for minimizing the impact of error correction when it is needed. The non-volatile memory system then-generates host data by executing a low density parity check (LDPC) iterative decode on the hard data bits and the syndrome bits for increasing the reliability of the user data without unnecessarily impacting capacity or performance.

Certain embodiments of the invention have other steps or elements in addition to or in place of those mentioned above. The steps or elements will become apparent to those skilled in the art from a reading of the following detailed description when taken with reference to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a block diagram of a non-volatile memory system with error correction mechanism in an embodiment of the present invention.

FIG. **2** is a detailed block diagram of an exemplary read path of the non-volatile memory system of FIG. **1**.

FIG. **3** is a control flow for a first embodiment of the non-volatile memory system of FIG. **1**.

FIG. **4** is a control flow for a second embodiment of the non-volatile memory system of FIG. **1**.

FIG. **5** is a control flow for a third embodiment of the non-volatile memory system of FIG. **1**.

FIG. **6** is an exemplary timing diagram of the power used for data retrieval processes of the non-volatile memory system of FIG. **1**.

FIG. **7** is a flow chart of a method of operation of a non-volatile memory system in a further embodiment of the present invention.

DETAILED DESCRIPTION

The following embodiments are described in sufficient detail to enable those skilled in the art to make and use the claimed invention. It is to be understood that other embodiments would be evident based on the present disclosure, and that system, process, or mechanical changes may be made without departing from the scope of the claimed invention.

In the following description, numerous specific details are given to provide a thorough understanding of the invention. However, it will be apparent that the invention may be practiced without these specific details. In order to simplify the disclosure, some well-known circuits, system configurations, and process steps are not disclosed in detail.

The drawings showing embodiments of the system may be drawn not to scale. Similarly, although the views in the drawings for ease of description generally show similar orientations, this depiction in the figures is arbitrary for the most part. Generally, the invention can be operated in any orientation.

The same numbers are used in all the drawing FIGs. to relate to the same elements. The embodiments have been numbered first embodiment, second embodiment, etc. as a matter of descriptive convenience and are not intended to have any other significance or provide limitations for the present invention.

Various embodiments described here include a new approach to improving data integrity in a non-volatile memory system. This approach includes a method including:

accessing a non-volatile memory cell for retrieving hard data bits; generating soft information by capturing a reliability of the hard data bits; calculating syndrome bits by applying a lossy compression to the soft information; and generating a host data by executing a low density parity check (LDPC) iterative decode on the hard data bits and the syndrome bits.

The present invention provides a non-volatile memory system, including: a non-volatile memory cell, coupled to a destination register, for retrieving hard data bits; a soft information module, coupled to the destination register, for capturing a reliability of the hard data bits; a lossy compression module, coupled to the soft information module, for calculating syndrome bits; and an error correction module, coupled to the lossy compression module, for generating a host data by executing a low density parity check (LDPC) iterative decode on the hard data bits and the syndrome bits.

Referring now to FIG. **1**, therein is shown a block diagram of a non-volatile memory system **100** with error correction mechanism in an embodiment of the present invention. The block diagram of the non-volatile memory system **100** depicts a host data bus **104**, a command interface **106**, and a system power interface **110** coupled to a storage power manager **112**.

The storage power manager **112** can provide operational power and alerts to a controller module **114** and an array **116** of a non-volatile memory device **118**. The non-volatile memory device **118** can be NAND flash memory, single-level cell (SLC) flash memory, or multi-level cell (MLC) flash memory. The array **116** of the non-volatile memory device **118** can be coupled through a flash data bus **115** to the controller module **114**. The controller module **114** can be a hardware module having a processor module **120**, a processor memory module **122**, a flash interface controller **124**, a non-volatile memory controller **126**, and an error correction module **128**, such as a low density parity check (LDPC) decoder module.

The processor module **120** can perform maintenance and support tasks for the non-volatile memory system **100**. The processor memory module **122** can be coupled to the processor module **120** to operate as data cache, temporary storage, instruction storage, and interface state memory.

The flash interface controller **124** is a hardware structure coupled between the flash data bus **115**, and the error correction module **128**. The flash interface controller **124** can manage the transfer of the hard data bits read from the non-volatile memory device **118**. The hardware for the flash interface controller **124** can be a multiplexed structure that uses the flash data bus **115** to transfer the either the hard data bits read from the non-volatile memory device **118** or soft correction bits used by the error correction module **128**.

Data written to the non-volatile memory device **118** can be randomized for either security reasons or for endurance and retention requirements. The resulting data is known to have high entropy, such as 50% 1's and 50% 0's. The number of data bits written at a value of 1 or 0 can be predicted. As the non-volatile memory device **118** ages a ratio of the number of 1's to 0's will change due to charge depletion in the non-volatile memory device **118**. The charge depletion can occur due to the age of the data or an excessive number of reads of the data in the non-volatile memory device **118**.

In normal operation, spurious data errors can be corrected by the error correction module **128** without re-reading the erroneous data blocks. As the charge is depleted with a given threshold voltage (V_{th}), the ratio of the number of 1's to 0's can change. As the number of bit errors increases, additional levels of the soft correction bits can be needed by the error correction module **128** to provide corrected data.

The processor module **120** can detect the increasing use of the error correction module **128**. The processor module **120** can configure the flash interface controller **124** in order to invoke an increased number of the soft correction bits to the error correction module **128**. The output of the flash interface controller **124** can steer the hard data bits to the error correction module **128** and the soft correction bits to additional logic to aid in the correction process.

It is understood that the activation of the flash interface controller **124** can be part of an error recovery process or as part of a continuous monitoring of the condition of the data within the non-volatile memory device **118**. It is further understood that the adjustments of the threshold voltage (V_{th}) can be implemented to automatically apply to the non-volatile memory device **118** without intervention of the processor module **120**.

It has been discovered that the flash data controller **124** can aid in the correction of the hard data read from the non-volatile memory device **118** while minimizing the use of additional power and latency. It has further been discovered that the flash interface controller **124** can quickly assist in the identification of suspect bits in the hard data read from the non-volatile memory device **118** while minimizing the utilization of additional power and latency.

Referring now to FIG. **2**, therein is shown a detailed block diagram of an exemplary read path of the non-volatile memory system **100** of FIG. **1**. The detailed block diagram of the exemplary read path **201** of the non-volatile memory system **100** depicts the non-volatile memory device **118** coupled to the controller module **114** by the flash data bus **115**.

The non-volatile memory device **118** can include a number of non-volatile memory cells **202** coupled through a read bus **204** to a destination register **206**. The destination register **206** can include a first read register **208** and a second read register **210**. The first read register **208** and the second read register **210** can each receive the hard data bits from the read bus **204** at a different threshold voltage (V_{TH}) (not shown). The subsequent reads of the same data location using different levels of the threshold voltage can load the same data in the first read register **208** and the second read register **210** or it can cause some of the bits to change value. In the event none of the bits change, the reliability of all of the bits is known with high confidence.

An output of the destination register **206** can be hard data bits **212**. If the confidence in all of the hard data bits **212** is high, the code word, represented by the hard data bits **212**, can be correctly decoded by the error correction module **128** and the results are presented on the host data bus **104**. It is understood that while the hard data bits **212** are shown as a single line, the number of the hard data bits **212**, represented in a code word decoded by the error correction module **128**, can be 8 bits, 16 bits, 32 bits, 64 bits or some other number of bits limited only by the design of the controller module **114** and the non-volatile memory device **118**.

In the event the bit values in the first read register **208** and the second read register **210** are different, the individual bits that change value are suspect and can be flagged as having a probability of being the incorrect value as transferred in the hard data bits **212**. A reliability logic module **214** can compare changes of the data bits from the first read register **208**, loaded at a first threshold voltage (V_{TH}) and the second read register **210**, loaded at a second threshold voltage (V_{TH}), based on the change in threshold voltage (V_{TH}) applied to the non-volatile memory cell **202**. The reliability logic module **214** can be coupled to a soft information module **216** for generation of soft information **218** indicating the probability

of the correctness of the hard data bits **212**. The soft information module **216** can provide an offset pointer (not shown) for accessing selected portions of the soft information **218**.

It is understood that the destination register **206** can have additional registers beyond the first read register **208** and the second read register **210** in order to capture additional information about the number of bits that change due to changes in the threshold voltage (V_{TH}). It is also understood that the reliability logic module **214** can be integrated into the destination register **206**. The reliability logic module **214** is shown separately to clarify the function.

A lossy compression module **220** can perform a lossy compression of the soft information **218**. The lossy compression module **220** can reduce the size of the soft information **218** by selecting a subset of the soft information **218** for transfer to the controller module **114**. The lossy compression module **220** can reduce the transfer time and power required to convey the soft information **218** to the controller module **114**. By way of an example, the lossy compression module can be structured to transfer only every N^{th} bit of the soft information **218**, which requires $(1/N)^{th}$ of the time to complete the transfer and $(1/N)^{th}$ of the energy that would be required to transfer all of the bits of the soft information **218**.

The lossy compression module **220** can provide a syndrome bits **222** that reflects the lossy compression of the soft information **218**. The syndrome bits **222** can be coupled to a multiplexer **224** for transferring the syndrome bits **222** across the flash data bus **115**. A selection controller **226** can control the data select line **228** in order to switch the multiplexer between the hard data bits **212** and the syndrome bits **222**. The output of the multiplexer **224** is the flash data bus **115**, which is coupled to a demultiplexer **230** for steering the hard data bits **212** to the error correction module **128** and the syndrome bits **222** to a decompression module **232**.

The selection controller **226** can maintain the selection of the hard data bits **212** until a code word is not correctly decoded. Upon detecting a decode error from the error correction module **128**, the selection controller **226** can select the syndrome bits **222**. The syndrome bits **222** is generated during the decode process of the error correction module **128** and is waiting for transmission when the selection controller **226** switches the data select line **228**.

The decompression module **232** can perform an iterative cycle decompression of the syndrome bits **222**. The decompression module **232** can accept a second transfer of the syndrome bits **222** without discarding the first transfer. A compute log likelihood ratio (LLR) module **234** can calculate the probability of an individual bit being in error. The compute LLR module **234** can be coupled to the error correction module **128** for aiding in the LDPC decode of the code word.

The compute LLR module **234** can calculate the probability that bits addressed by the decompression module **232** contain an incorrectly read bit. The compute LLR module **234** can be a hardware accelerator, combinational logic, a microprogrammed hardware sequencer, or other fast calculating combination. Probability bits **236**, calculated by the compute LLR module **234**, can be applied to the error correction module **128** for executing an LDPC iterative decode process of the code word represented by the hard data bits **212**. Any of the bits that are not reflected in the probability bits **236** is assumed to be a valid bit. If a subsequent LDPC decode performed by the error correction module **128** is unsuccessful, additional sets of the syndrome bits **222** can be iteratively transferred to the decompression module **232**, which will add them to the syndrome bits **222** previously transferred in order to provide additional of the probability bits **236** and increase the bit correction capability to the error correction module **128**.

It has been discovered that the non-volatile memory system **100** of FIG. **1** can minimize the time and energy required to perform correction of the hard data bits **212** when the error correction module **128** is unable to correctly decode a code word. The minimization of the time and energy can be provided by the lossy compression module **220**, which generates the syndrome bits **222** having a shorter length than the entire length of the soft information **218**.

Referring now to FIG. **3**, therein is shown a control flow **301** for a first embodiment of the non-volatile memory system **100** of FIG. **1**. The control flow **301** for a first embodiment of the non-volatile memory system **100** depicts an error detected module **302** that indicates the hard data bits **212** of FIG. **2** were not decoded correctly by the error correction module **128** of FIG. **1**. A modulus number N can be selected by the controller module **114** of FIG. **1** and configured into the lossy compression module **220** of FIG. **2**. A start transfer bit K can be initialized to a zero value for the start of a correction process.

A transmit soft information module **304** will cause the selection controller **226** of FIG. **2** to switch the data select line **228** of FIG. **2** to allow the syndrome bits **222** of FIG. **2** onto the flash data bus **115** of FIG. **1** and into the decompression module **232** of FIG. **2**. The lossy compression module **220** will transfer every N^{th} bit starting with the K^{th} bit. An initial transfer of the syndrome bits **222** of FIG. **2** will include bit **0**, bit N, bit **2**N, bit **3**N, etc.

The syndrome bits **222** can be gated through the multiplexer **224** of FIG. **2**, the flash data bus **115** and the demultiplexer **230** of FIG. **2** to the decompression module **232**. The decompression module **232** can register the values of the syndrome bits **222** in a bit appropriate location for reconstructing the soft information **218** of FIG. **2**. The decompression module **232** provides the registered bits to the calculate LLR module **234**, which calculates the probability bits **236** for use in the LDPC decode process performed by the error correction module **128**.

A perform soft decoding module **306** can signal the error correction module **128** to perform the iterative decoding of the code word represented by the hard data bits **212** and the probability bits **236**. A check decode successful module **308** can determine whether the iterative soft decode yielded a valid code word. It the iterative soft decode was successful a read next data module **310** can be invoked. The read next data module **310** can switch the data select line **228** in order to gate the contents of the destination register **206** of FIG. **2**, including the hard data bits **212**.

If the check decode successful module **308** determines that the error correction module **128** was unsuccessful in the iterative soft decode, an increment start bit location module **312** can cause the lossy compression module **220** to index the starting bit location to K+1. This indexing would cause the syndrome bits **222** to represent bit **1**, bit N+1, bit **2**N+1, bit **3**N+1, etc.

A maximum count check module **314** can determine whether the maximum number of the syndrome bits **222** has been transferred, or the iterative soft decoding has reached a programmatic maximum number of attempts. When the value of K is equal to N, all of the soft information **218** would have been transferred. If the maximum count check module **314** determines that the maximum count has not been reached, the transmit soft information module **304** can retrieve the next set of the syndrome bits **222** for another attempt of the iterative soft decode can be attempted. If the transmit soft information module **304** determines the maximum count has been reached, an error flag can be set in the controller module **114** and the read next data module **310** can be invoked to re-read

the erroneous data as part of an error recovery process or it can increment the address in the non-volatile memory device **118** of FIG. **1** to read the next code word.

It has been discovered that transfer of the syndrome bits **222** from the lossy compression module **220** can correct the vast majority of the unsuccessful decode of the code word by the error correction module **118**. Due to the monitoring and exchange of bad pages within the non-volatile memory cells **202**, most of the data will be read with high reliability. As the non-volatile memory device **118** ages an increased number of single and double bit errors can be detected. The correction of these errors can be performed by the non-volatile memory system **100** while still utilizing less time and less energy than would be required by other error correction mechanisms.

By way of an example, with the value of N=4, every 4^{th} bit of the soft information **218** can be used to perform the iterative soft decode an example read of the hard data bits **212**, the soft information **218**, the syndrome bits **222** represented by every 4^{th} bit of the soft information **218**.

TABLE 1

a value of 1 in the soft information means the bit is suspect

Hard Data Bits:	1	0	1	1	0	0	0	1	0	1	1	1	0	1	0	1	0
Soft Information	0	0	0	0	1	0	0	1	0	0	0	0	1	1	1	0	0
Syndrome Bits	0				1				0				1				0
LLR (all soft info)	15	−15	15	15	−3	−15	−15	3	−15	15	15	15	−3	3	−3	15	−15
LLR (X Soft info)	15	−11	11	11	−3	−11	−11	11	−15	11	11	11	−3	11	−11	11	−15

The LLR values show the probability bits **236** value with all of the soft information **218** transferred. A value of 15 is a very confident 1 and a value of −15 is a very confident 0. The lower the absolute number of the probability the less confidence is conveyed. In the example the LLR for X of the soft information **218** has the correct values for the syndrome bits **222** that are available and the remaining bits are assumed to most likely be correct. As more of the syndrome bits **222** become available, more of the suspect bits will be identified and can be corrected. In the example above a LLR value of −3 represents a weak 0 and a LLR value of 3 represents a weak 1. The error correction module **128** can iteratively reverse the value of the low confidence bits during the iterative soft decode process in order to correct the code word.

Referring now to FIG. **4**, therein is shown a control flow **401** for a second embodiment of the non-volatile memory system **100** of FIG. **1**. The control flow **401** depicts an error detected module **402** that indicates the hard data bits **212** of FIG. **2** were not decoded correctly by the error correction module **128** of FIG. **1**. Modulus numbers M and N can be selected by the controller module **114** of FIG. **1** and configured into the lossy compression module **220** of FIG. **2**. The value of M can be a span of bits that are referenced together by a single soft information value. The value of N can be a divisor of the code word that would determine the reduction in time and power for performing the iterative correction process. A start transfer bit K can be initialized to a zero value for the start of a correction process.

The value of M represents a span of the hard data bits **212** that are reflected in the soft information **218** provided by the lossy compression module **220**. The value of M must be greater than or equal to 2. The syndrome bits **222** can convey the minimum reliability across the span of M bits, the average reliability across the span of M bits, or the median value of the reliability across the span of M bits. Each of the different meanings of M would require a different LDPC decode strategy to be implemented. In this description, the syndrome bits **222** convey the minimum reliability across the span of M bits.

By way of an example, the soft information **218** can include 3 bits for each of the hard data bits **212**. The most significant bit can indicate the value of the detected bit as either a 1 or a 0. The remaining two bits can indicate the confidence that the value of the detected bit is correct. The confidence bits can represent values of 0-3, where a value of 3 indicates high confidence that the detected bit is correct and a value of 0 indicates low confidence.

By way of an example, with the value of M and N=4, every 4^{th} bit of the soft information **218** can represent the lowest confidence across the span of 4 bits, This information can be used to perform the iterative soft decode an example read of the hard data bits **212**, the soft information **218**, the syndrome bits **222** represented by every 4^{th} bit of the soft information **218**.

TABLE 2

Each span of 4 bits of Soft information have the same numerical confidence as the lowest confidence in the span.

Hard Data Bits:	1	0	1	1	0	0	0	1	0	1	1	1	0	1	0	1	0
Soft Information	3	3	2	0	3	2	3	2	3	3	3	3	1	2	1	3	0
Syndrome bits	0				2				3				1				0
LLR (all soft info)	15	−15	11	1	−15	−11	−15	11	−15	15	15	15	−5	11	−5	15	−1
LLR (1/4 Soft info)	1	−1	1	1	−11	−11	−11	11	−15	15	15	15	−5	5	−5	5	−1

A transmit soft information span module **404** will cause the selection controller **226** of FIG. **2** to switch the data select line **228** of FIG. **2** to allow the syndrome bits **222** of FIG. **2** onto the flash data bus **115** of FIG. **1** and into the decompression module **232** of FIG. **2**. The lossy compression module **220** will transfer the syndrome bits **222** for each of the spans M starting with the K^{th} bit. An initial transfer of the syndrome bits **222** will include M**1** covering bits **0** through M−1, M**2** covering bits M through **2**M−1, M**3** covering **2**M through **3**M−1, etc.

A perform soft decoding module **406** can signal the error correction module **128** to perform the LDPC iterative decoding of the code word represented by the hard data bits **212** and the probability bits **236** of FIG. **2**. A check decode successful module **408** can determine whether the iterative soft decode yielded a valid code word. If the iterative soft decode was

successful a read next data module **410** can be invoked. The read next data module **410** can switch the data select line **228** in order to gate the contents of the destination register **206** of FIG. **2**, including the hard data bits **212**.

If the check decode successful module **408** determines that the error correction module **128** was unsuccessful in the iterative soft decode, a maximum count check module **412** can determine whether the maximum number of the syndrome bits **222** has been transferred, or the iterative soft decoding has reached a programmatic maximum number of attempts. When the value of K is equal to N, all of the soft information **218** would have been transferred. If the maximum count check module **412** determines that the maximum count has not been reached, a transmit soft information module **414** can retrieve a set of the syndrome bits **222** for another attempt of the iterative soft decode can occur. The transmit soft information module **414** will cause the selection controller **226** of FIG. **2** to switch the data select line **228** of FIG. **2** to allow the syndrome bits **222** of FIG. **2** onto the flash data bus **115** of FIG. **1** and into the decompression module **232** of FIG. **2**. The lossy compression module **220** will transfer every N^{th} bit starting with the K^{th} bit. The transfer of the syndrome bits **222** of FIG. **2** will include bit **0**, bit N, bit **2**N, bit **3**N, etc.

If the maximum count check module **412** determines that the maximum count has been reached, an error flag can be set in the controller module **114** of FIG. **1** and the read next data module **410** can be invoked to re-read the erroneous data as part of an error recovery process or it can increment the address in the non-volatile memory device **118** of FIG. **1** to read the next code word.

An increment start bit location module **416** can cause the lossy compression module **220** to index the starting bit location to K+1. This indexing would cause the syndrome bits **222** to represent bit **1**, bit N+1, bit **2**N+1, bit **3**N+1, etc. in preparation for the next transfer of the syndrome bits **222**. The error correction module **128** can gain an understanding of the distribution of the unreliable bit locations from the initial syndrome bits **222** covering the spans of M bits. When the additional syndrome bits **222** are added to the LDPC iterative decode process a quick clarification of the suspect bits can lead to a valid decode of the code word.

It has been discovered that the use of the syndrome bits **222** that reflect the lowest confidence in a span of the hard data bits **212** can allow the error correction module **128** to concentrate the LDPC iterative decode process on the spans that have the lowest confidence. Since most of the hard data bits **212** are highly reliable knowing which spans have suspected bits can resolve the decode without additional information. If additional information is needed to resolve the code word, the syndrome bits **222** can be transferred in order to complete the LDPC iterative decode process.

Referring now to FIG. **5**, therein is shown a control flow **501** for a third embodiment of the non-volatile memory system **100** of FIG. **1**. A variable rate code for sharing soft information between the non-volatile memory device **118** of FIG. **1** and the error correction module **128** of FIG. **1** can improve the efficiency of the LDPC iterative decode process. To be efficient, bit patterns that repeat frequently should be represented with short codes for the syndrome bits **222** of FIG. **2**, and uncommon bit sequences can be represented with long codes for the syndrome bits **222** since they occur so infrequently.

TABLE 3

Sample code words with a probability of occurrence.

N			8	
Prob of Unreliable Bit			0.01	
Prob of Reliable Bit			0.99	
# Unreliable bits/N	Prob of Occur	Syndrome bits	Syn Length	(Pr of occ) * Length
0	9.23E−01	0	1	9.23E−01
1	7.46E−02	10	2	1.49E−01
2	2.64E−03	110	3	7.91E−03
3	5.39E−05	1110	4	2.16E−04
4 or more	6.78E−07	11110	5	3.39E−06
		Avg soft Bits/data bit		0.135

In table 3, the "Prob of Occur" indicates the probability of occurrence of the number of bits being suspect within the span designated by N=8 for this example. The error correction module **128** would have a very high probability in excess of 90% of being able to perform the LDPC iterative decode process without using the syndrome bits **222** at all. By implementing the variable length of the syndrome bits **222**, the amount of time and energy used for correctly decoding the hard data bits **212** can be minimized.

The lossy compression module **220** can provide a variable length for the syndrome bits **222** per the values in table 3. The lossy compression module **220** can examine **8** of the bits of the soft information **218** at a time and construct the syndrome bits **222** to transfer in the lowest possible time and with the lowest possible energy utilized. With this strategy, each of the 8 bit spans in the code word can have the syndrome bits **222** terminated by a 0 value. By counting the preceding number of 1's in the syndrome bits **222**, the error correction module **128** can know how many of the hard data bits **212** are possibly in error for each 8 bit span.

The control flow **501** depicts an error detected module **502** that indicates the hard data bits **212** of FIG. **2** were not decoded correctly by the error correction module **128** of FIG. **1**. Modulus number N can be selected by the controller module **114** of FIG. **1** and configured into the lossy compression module **220** of FIG. **2**. The value of N can be a span of bits that are referenced together by a single soft information value. A start transfer bit K can be initialized to a zero value for the start of a correction process.

A transmit soft information module **504** will cause the selection controller **226** of FIG. **2** to switch the data select line **228** of FIG. **2** to allow the syndrome bits **222** of FIG. **2** onto the flash data bus **115** of FIG. **1** and into the decompression module **232** of FIG. **2**. The lossy compression module **220** will transfer an appropriate set of the syndrome bits **222** to match the number of the unreliable bits as listed in table 3.

The syndrome bits **222** can be gated through the multiplexer **224** of FIG. **2**, the flash data bus **115** and the demultiplexer **230** of FIG. **2** to the decompression module **232**. The decompression module **232** can register the values of the syndrome bits **222** in a bit appropriate location for reconstructing the soft information **218** of FIG. **2**. The decompression module **232** provides the registered bits to the calculate LLR module **234**, which calculates the probability bits **236** for use in the LDPC iterative decode process performed by the error correction module **128**.

In order to clarify the description, it is assumed that the number of the hard data bits **212** is limited to 8 for this example. It is understood that the algorithm can be expanded to any bus width for the hard data bits **212**.

A zero bad bits check **506** can verify whether there are no unreliable bits indicated in the soft information **218**. If the zero bad bits check **506** determines that none of the hard data bits **212** are unreliable, a send syndrome **1** module **508** can transfer the syndrome bits **222** from table 3 to the decompression module **232**.

A perform soft decode module **510** can trigger the error correction module **128** to perform the LDPC iterative decode process again. A successful decode check **512** can verify that the LDPC iterative decode process was successful. If the LDPC iterative decode process was successful, a read next data module **514** can switch the data select line **228** in order to gate the contents of the destination register **206** of FIG. **2**, including the hard data bits **212** to access the next location in the non-volatile memory device **118**.

If the successful decode check **512** verifies that the LDPC iterative decode process was not successful, an increment start bit location module **516** can increment K to K+1 in preparation for analyzing the soft information **218** again. A maximum count check module **518** can determine whether the maximum offset of K has been met. When the value of K is equal to K_MAX, all of the soft information **218** would have been transferred and the control flow can move to the read next data module **514**. An error flag can be set in the controller module **114** and the read next data module **310** can be invoked to re-read the erroneous data as part of an error recovery process or it can increment the address in the non-volatile memory device **118** of FIG. **1** to read the next code word.

If the maximum count check module **518** can determine that the maximum offset of K has not been met, an update soft information module **520** can initiate multiple reads of the non-volatile memory cells **202** with the threshold voltage (V_{TH}) offset. The update soft information module **520** can reload the destination register **206** of FIG. **2** in an attempt to correctly capture the hard data bits **212**. The control flow can then enter the zero bad bits check **506** for another attempt at determining the number of unreliable bits there are in the hard data bits **212**.

The control flow **501** can sort the soft information within the lossy compression module **220**. A one bad bit check **522** can look for a single unreliable bit in the hard data bits **212**. If a single unreliable bit is determined, a send syndrome **2** module **524** can send the syndrome bits **222** equal to "10", from table 3, to the decompression module **232** and the flow can invoke the LDPC iterative decode process in the error correction module **128**.

If the one bad bit check **522** does not find only the single bit to be unreliable, a two bad bit check **526** can look for two unreliable bits in the hard data bits **212**. If two unreliable bits are determined, a send syndrome **3** module **528** can send the syndrome bits **222** equal to "110", from table 3, to the decompression module **232** and the flow can invoke the LDPC iterative decode process in the error correction module **128**.

If the two bad bit check **526** does not find only two bits to be unreliable, a three bad bit check **530** can look for three unreliable bits in the hard data bits **212**. If three unreliable bits are determined, a send syndrome **4** module **532** can send the syndrome bits **222** equal to "1110", from table 3, to the decompression module **232** and the flow can invoke the LDPC iterative decode process in the error correction module **128**.

If the three bad bit check **530** does not find only three bits to be unreliable, a send syndrome **5** module **534** can send the syndrome bits **222** equal to "11110", from table 3, to the decompression module **232** and the flow can invoke the LDPC iterative decode process in the error correction module **128**. The send syndrome **5** module **534** can indicate that there are four or more unreliable bits in the hard data bits **212**.

By way of an example, a different variable length of the syndrome bits **222** can be defined, in contrast to the contents of table 3, to deliver a finer granularity in the designation of the location of the unreliable bits located in the hard data bits **212** in order to aid in the LDPC iterative decode process performed by the error correction module **128**. A unique version of the syndrome bits **222** can be specified for groups of bits in the hard data bits **212**. This approach can simplify the design of the error correction module **128** as well as speeding-up the LDPC iterative decode process. Since the vast majority of the hard data bits **212** are reliable, the infrequent occurrence of a transfer of the syndrome bits **222** maintains the goal of the non-volatile memory system **100** of FIG. **1** to reduce the time and energy required to correct the hard data bits **212** read from the non-volatile memory device **118**. It is understood that syndrome bits **222** are only transferred if an error is detected by the error correction module **128**.

An approach to provide additional detail of the location of the unreliable bits could be provided as shown in table 4 below.

TABLE 4

Finer granularity of unreliable bit location				
N			8	
	Prob of Unreliable Bit		0.01	
	Prob of Reliable Bit		0.99	
# Unreliable bits/N	Prob of Occur	Syndrome bits	Syn Length	(Pr of occ) * Length
0	9.23E−01	0	1	9.23E−01
1 in bits 0-1	1.86E−02	10	2	3.73E−02
1 in bits 2-3	1.86E−02	110	3	5.59E−02
1 in bits 4-5	1.86E−02	1110	4	7.46E−02
1 in bits 6-7	1.86E−02	11110	5	9.32E−02
2	2.64E−03	111110	6	1.58E−02
3	5.39E−05	1111110	7	3.78E−04
4 or more	6.78E−07	11111110	8	5.42E−06
		Avg soft Bits/data bit		0.150

By providing the finer granularity of the location of the unreliable bits in the hard data bits **212**, the correction time and complexity of the LDPC iterative decode process can be reduced. The design of the compute LLR module **234** of FIG. **2** can also be simplified to provide a more accurate probability of the correction.

The designation of additional combinations of the syndrome bits **222** can be extended to include the likely location of two bits that are unreliable by extending the syndrome bits **222** to cover different bit combinations. This approach can be extended to increase the complexity of the syndrome bits **222** while further simplifying the error correction module **128** and the compute LLR module **232**. By way of an implementation example without limiting the claimed invention, the lossy compression module **220** can use the soft information **218** to address a look-up table (not shown) that can be configured by the controller module **114** of FIG. **1** during initialization of the function to provide the syndrome bits **222**.

An expansion of the syndrome bits **222** to cover two bit errors can be demonstrated by the additional codes shown in table 5 below:

TABLE 5

Syndrome bits containing detailed location information and two bit locations				
N			8	
Prob of Unreliable Bit			0.01	
Prob of Reliable Bit			0.99	
# Unreliable bits/N	Prob of Occur	Syndrome bits	Syn Length	(Pr of occ) * Length
0	9.23E−01	0	1	9.23E−01
1 in bits 0-1	1.86E−02	10	2	3.73E−02
1 in bits 2-3	1.86E−02	110	3	5.59E−02
1 in bits 4-5	1.86E−02	1110	4	7.46E−02
1 in bits 6-7	1.86E−02	11110	5	9.32E−02
1 in bits 0-3, 1 in 4-7	1.51E−03	111110	6	9.04E−03
2 in bits 0-3	5.65E−04	1111110	7	3.95E−03
2 in bits 4-7	5.65E−04	11111110	8	4.52E−03
3 or more	5.39E−05	111111110	9	4.85E−04
4 or more	6.78E−07	1111111110	10	6.78E−06
		Avg Soft bits/data bit		0.150

More efficient codes, requiring more complex decoding and more complex encoding, can be constructed. An example of such codes is shown in Table 6. Note that while this code provides almost the same amount of information about the location of the erroneous bits as code 3, it results in fewer soft information bits per data bit. The syndrome bits **222** are constructed so that none codes of the syndrome bits **222** is part of the beginning of another of the codes of the syndrome bits **222**. To decode the stream of the syndrome bits **222**, the decoder counts the number of received bits until the received sequence is equivalent to one of the codes of the syndrome bits **222**. As it can be seen in Table 6, the reduced soft information bit transfer rate comes at the price of more decoding complexity.

TABLE 6

More complex Syndrome bits patterns provide fewer soft information bits per data bit.				
N			8	
Prob of Unreliable Bit			0.01	
Prob of Reliable Bit			0.99	
# Unreliable Bits/CW	Prob of Occur	Syndrome bits	Syn Length	(Pr of occ) * Length
0	9.23E−01	0	1	9.23E−01
1 in bits 0-1	1.86E−02	101	3	5.59E−02
1 in bits 2-3	1.86E−02	110	3	05.59E−02
1 in bits 4-5	1.86E−02	111	3	5.59E−02
1 in bits 6-7	1.86E−02	1000	4	7.46E−02
1 in bits 0-3 and 1 in bits 6-7	1.51E−08	10010	5	7.53E−03
2 in bits 0-3	5.65E−04	100111	6	3.39E−03
2 in bits 4-7	5.65E−04	1001100	7	3.95E−03
3 bits	5.39E−05	10011010	8	4.26E−04
4 bits or more	6.78E−07	10011011	8	5.53E−06
Average soft bits/data bit	0.1475			

It is understood that the tradeoff between encoder and decoder efficiency compared to bandwidth and energy efficiency is one that can be made between flash designers and LDPC decoder designers. As advances in semiconductor technology makes gates less expensive, it is likely that the transfer efficiency of the codes will become more important than simplicity of encoding and decoding.

By choosing longer codewords, such as N=10, or N=16, it is possible to create codes that are more efficient at the expense of having less accurate soft information. The loss of soft information accuracy causes the likelihood an uncorrectable sequence to increase. Ultimately, one can create more complex codes that convey more soft information to avoid increased probability of uncorrectable errors at the decoder output.

It has been discovered that the non-volatile memory system **100** can be configured to convey the syndrome bits **222** having a complexity that is suitable to the application requirements. In high reliability applications, more complex encoders and decoders can be used to convey increasingly accurate soft information to improve the reliability of the decoding process while minimizing the time and energy used during the LDPC iterative decode process. An approach to lessen the likelihood of the uncorrectable errors is to provide a programmable value of N allowing adjustment of the content of the syndrome bits **222** as necessary in the life cycle of the non-volatile memory system **100**.

Referring now to FIG. **6**, therein is shown an exemplary timing diagram **601** of the power used for data retrieval processes of the non-volatile memory system **100** of FIG. **1**. The exemplary timing diagram **601** depicts the power utilized by the non-volatile memory system **100** to retrieve the hard data bits **212** of FIG. **2** and perform the LDPC iterative decode process to correctly decode the host data **104** of FIG. **1**. The read access **602**, of the non-volatile memory cells **202** of FIG. **2**, can take 40-60 microseconds for storing the contents of the non-volatile memory cells **202** in the first read register **208** of FIG. **2** and the second read register **210** of FIG. **2**. During the read access **602** the reliability logic **214** of FIG. **2** can generate the soft information **218** of FIG. **2** and the syndrome bits **222** of FIG. **2**. The transfer **604** of the hard data bits **212** of FIG. **2** can from the destination register **206** of FIG. **2** to the error correction module **128** of FIG. **1** can take 45 microseconds.

By utilizing the variable length of the syndrome bits **222**, of the non-volatile memory system **100**, the syndrome bits transfer **606** required for the LDPC iterative decode process can be between 6 and 10 micro-seconds. This can be favorably compared to the transfer of the total content of the soft information **218** which would take the same 45 microseconds of time and energy as the transfer **604** of the hard bits **212**. An energy saving duration **608** can be between 35 and 39 microseconds. The efficiencies provided by the non-volatile memory system **100** can improve bandwidth and energy utilization while maintaining a robust error correction capability.

Referring now to FIG. **7**, therein is shown a flow chart of a method **700** of operation of a non-volatile memory system in a further embodiment of the present invention. The method **700** includes: accessing a non-volatile memory cell for retrieving hard data bits in a block **702**; generating soft information by capturing a reliability of the hard data bits in a block **704**; calculating syndrome bits by applying a lossy compression to the soft information in a block **706**; and generating a host data by executing a low density parity check (LDPC) iterative decode on the hard data bits and the syndrome bits in a block **708**.

The resulting method, process, apparatus, device, product, and/or system is straightforward, cost-effective, uncomplicated, highly versatile, accurate, sensitive, and effective, and can be implemented by adapting known components for ready, efficient, and economical manufacturing, application, and utilization.

Another important aspect of the present invention is that it valuably supports and services the historical trend of reducing costs, simplifying systems, and increasing performance.

These and other valuable aspects of the present invention consequently further the state of the technology to at least the next level.

While the invention has been described in conjunction with a specific best mode, it is to be understood that many alternatives, modifications, and variations will be apparent to those skilled in the art in light of the aforegoing description. Accordingly, it is intended to embrace all such alternatives, modifications, and variations that fall within the scope of the included claims. All matters hithertofore set forth herein or shown in the accompanying drawings are to be interpreted in an illustrative and non-limiting sense.

What is claimed is:

1. A method for improving data integrity in a non-volatile memory system comprising:

accessing non-volatile memory cells for retrieving hard data bits;

decoding the hard data bits; and

in response to a determination that decoding the hard data bits was not successful:

generating soft information by capturing a reliability of the hard data bits, wherein generating the soft information includes loading a first read register with values of the hard data bits read using a first threshold voltage and loading a second read register, distinct from the first register, with values of the hard data bits read using a second threshold voltage, and comparing the contents of the first read register with the contents of the second read register;

delivering the soft information and values from at least one of the first read register and second read register to an error correction module via a multiplexer;

calculating syndrome bits by applying a lossy compression to the soft information; and

generating host data by executing a low density parity check (LDPC) iterative decode on the hard data bits and the syndrome bits.

2. The method as claimed in claim **1** further comprising calculating probability bits from the syndrome bits.

3. The method as claimed in claim **1** wherein calculating the syndrome bits includes determining a number of unreliable bits and sending a syndrome **1** to a decompression module.

4. The method as claimed in claim **1** wherein executing the low density parity check (LDPC) iterative decode on the hard data bits and the syndrome bits includes calculating probability bits from the syndrome bits.

5. The method as claimed in claim **1** further comprising performing an iterative cycle decompression of the syndrome bits by transferring a second set of the syndrome bits.

6. A non-volatile memory system comprising:

non-volatile memory cells, coupled to a destination register, for retrieving hard data bits, wherein the destination register includes a first read register, for loading hard data bits using a first threshold voltage, and a second read register, for loading values of the hard data bits read using a second threshold voltage;

a reliability logic module, coupled to the destination register, for comparing the contents of the first read register with the contents of the second read register;

a soft information module, coupled to the reliability logic module, for generating soft information by capturing a reliability of the hard data bits;

a lossy compression module, coupled to the soft information module, for calculating syndrome bits by applying a lossy compression to the soft information;

an error correction module, coupled to the lossy compression module, for generating host data by executing a low density parity check (LDPC) iterative decode on the hard data bits and the syndrome bits; and

a multiplexer coupling at least one of the first read register and second read register to the error correction module;

wherein the soft information module, lossy compression module and error correction module are configured to generate the soft information, calculate the syndrome bits and generate host data by executing the low density parity check iterative decode on the hard data bits and the syndrome bits in response to a determination that decoding the hard data bits was not successful.

7. The system as claimed in claim **6** further comprising a compute log likelihood ratio (LLR) module, coupled to the lossy compression module, for calculating probability bits from the syndrome bits.

8. The system as claimed in claim **6** wherein the lossy compression module, coupled to a multiplexer, is further for determining a number of unreliable bits and sending a syndrome to a decompression module.

9. The system as claimed in claim **6** wherein the error correction module, coupled to the lossy compression module, for generating host data includes a compute log likelihood ratio (LLR) module between the error correction module and the lossy compression module for calculating probability bits from the syndrome bits.

10. The system as claimed in claim **6** further comprising a decompression module configured to perform an iterative cycle decompression of the syndrome bits by transferring a second set of the syndrome bits having an incremented start location.

11. A non-volatile memory system comprising:

a non-volatile memory device that includes:

non-volatile memory cells having hard data bits;

a destination register, coupled to the non-volatile memory cells, for retrieving the hard data bits, wherein the destination register includes a first read register, for loading hard data bits using a first threshold voltage, and a second read register, for loading values of the hard data bits read using a second threshold voltage;

a reliability logic module, coupled to the destination register, for comparing the contents of the first read register with the contents of the second read register;

a soft information module, coupled to the reliability logic module, for generating soft information by capturing a reliability of the hard data bits; and

a lossy compression module, coupled to the soft information module, for calculating syndrome bits by applying a lossy compression to the soft information; and

a controller module, coupled to the non-volatile memory device, the controller module including an error correction module for generating host data by executing a low density parity check (LDPC) iterative decode on the hard data bits and the syndrome bits;

the non-volatile memory device further including a multiplexer coupling at least one of the first read register and second read register to the error correction module;

wherein the soft information module, lossy compression module and error correction module are configured to generate the soft information, calculate the syndrome bits and generate host data by executing the low density parity check iterative decode on the hard data bits and the syndrome bits in response to a determination that decoding the hard data bits was not successful.

12. The system as claimed in claim 11 wherein the controller module further includes a compute log likelihood ratio (LLR) module for calculating probability bits from the syndrome bits.

13. The system as claimed in claim 11 wherein:

the non-volatile memory device having the lossy compression module, coupled to the soft information module, is further for determining a number of unreliable bits and sending a syndrome; and

the controller module further includes a decompression module for decompressing the syndrome.

14. The system as claimed in claim 11 wherein the controller module includes a compute log likelihood ratio (LLR) module for calculating probability bits, from the syndrome bits, for the error correction module.

15. The system as claimed in claim 11 wherein:

the non-volatile memory device includes:

a reliability logic module, coupled to the destination register, for calculating a soft information, and

a multiplexer, coupled to the lossy compression module and the destination register, for transferring the hard data bits and the syndrome bits on a flash data bus; and

the controller module includes a demultiplexer, coupled to the flash data bus, for separating the hard data bits and the syndrome bits from the flash data bus.

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